# VHF push-pull power MOS transistor

#### **FEATURES**

- · High power gain
- · Easy power control
- · Good thermal stability
- Gold metallization ensures excellent reliability.

## DESCRIPTION

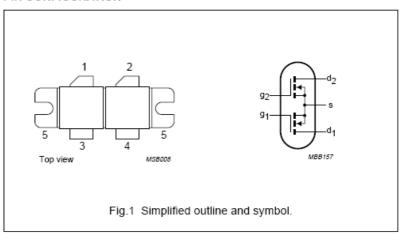
Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

# PINNING - SOT262 A1

PIN	DESCRIPTION	
1	drain 1	
2	drain 2	
3	gate 1	
4	gate 2	
5	source	

#### PIN CONFIGURATION



#### CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## WARNING

#### Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance at Th = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>P</sub> (dB)	η <sub>D</sub> (%)
class-AB	225	28	300	> 10	> 55
	175	28	300	typ. 13	typ. 67

# **ELEFLOW TECHNOLOGIES**

www.eleflow.com

## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134). Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		-	65	٧
±V <sub>GS</sub>	gate-source voltage		-	20	٧
I <sub>D</sub>	DC drain current		-	25	Α
P <sub>tot</sub>	total power dissipation	up to T <sub>mb</sub> = 25 °C total device; both sections equally loaded	-	500	W
T <sub>stg</sub>	storage temperature		-65	150	°C

## THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
R <sub>th j-mb</sub>	thermal resistance from junction to mounting base	total device; both sections equally loaded.	0.35 K/W
R <sub>th mb-h</sub>	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	0.15 K/W

